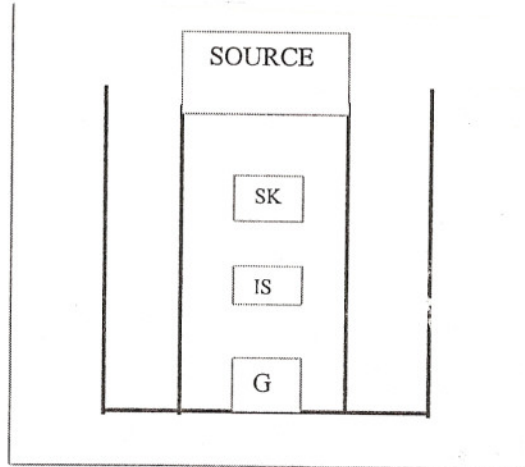




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



SK = SOURCE KELVIN
IS = CURRENT SENSE

SOURCE 0.039" X 0.030"; GATE 0.021" X 0.015"

Topside Metal: Al
Backside: Cr Ni Ag
Backside Potential: Drain
Mask Ref:
Bond Pads : .004"

APPROVED BY: CB
MFG: IR

DIE SIZE : .227" x .171"
THICKNESS: .020"

DATE: 2/7/01
P/N: IRCC130BV

DG 10.1.2
Rev A 3-4-99